This Listing of Claims will replace all prior versions or listings of claims in this application.

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor memory device operable in a merged data input/output pin (DQ) test mode, comprising:

a first path circuit receiving a first data bit, a second single data rate (SDR) signal, and a first transmission signal pair and producing a first path output signal and including a first switching element controlled by the second single data rate signal;

a second path circuit receiving a second data bit, a first single data rate signal, and a second transmission signal pair and producing a second path output signal and including a second switching element controlled by the first single data rate signal; and

a merged output generator configured to generate a merged data bit based on the first path output signal and the second path output signal having a single data rate (SDR) pattern and/or a dual data rate (DDR) pattern, as determined by the first single data rate signal fed to the second switching element and the second single data rate signal fed to the first switching element and the first and second transmission signal pairs.

2. (Canceled)

3. (Previously Presented) The semiconductor memory device of claim 1, further comprising a control signal generator configured to generate the first and second SDR signals fed to the second path circuit and the first path circuit, respectively, and to generate the first and second transmission signal pairs.

4. (Canceled)

5. (Previously Presented) The semiconductor memory device of claim 3, wherein the control signal generator comprises:

a first NOR gate receiving first and second output clock signals;

first, second, and third inverters, wherein outputs of the second and third inverters are the first transmission signal pair;

a second NOR gate receiving third and fourth output clock signals;

fourth, fifth, and sixth inverters, wherein outputs of the fifth and sixth inverters are the second transmission signal pair;

a first NAND gate generating the second SDR signal; and

a second NAND gate generating the first SDR signal.

6. (Original) The semiconductor memory device of claim 5, wherein the first SDR signal is generated in response to a main signal of the first transmission signal pair and a complementary signal of the second transmission signal pair.

7. (Original) The semiconductor memory device of claim 5, wherein the second SDR signal is generated in response to a complementary signal of the first transmission signal pair and a main signal of the second transmission signal pair.

8. (Previously Presented) The semiconductor memory device of claim 3, wherein the first path circuit comprises:

a first inverter receiving a merging flag signal;

a NOR gate receiving an output of the first inverter and the first data bit;

a transmission gate transferring an output of the NOR gate in response to the first transmission signal pair;

a PMOS transistor forming the first switching element for connecting a power supply to the transmission gate in response to the second SDR signal;

a latch holding a voltage level of an output node of the transmission gate; and

a second inverter converting an output of the latch into the first path output signal.

9. (Original) The semiconductor memory device of claim 8, wherein the first data path circuit propagates the first data bit generated at a first edge of a clock signal.

10. (Original) The semiconductor memory device of claim 8, wherein the first path circuit further comprises an NMOS transistor resetting the output node of the transmission gate in response to a reset signal.

11. (Previously Presented) The semiconductor memory device of claim 3, wherein the second path circuit comprises:

a first inverter receiving a merging flag signal;

a NOR gate receiving an output of the first inverter and the second data bit;

a transmission gate transferring an output of the NOR gate in response to the second transmission signal pair;

a PMOS transistor forming the second switching element for connecting a power supply to the transmission gate in response to the first SDR signal;

a latch holding a voltage level of an output node of the transmission gate; and

a second inverter converting an output of the latch into the second path output signal.

12. (Original) The semiconductor memory device of claim 11, wherein the second data path circuit propagates the first data bit generated at a second edge of a clock signal.

13. (Original) The semiconductor memory device of claim 11, wherein the second path circuit further comprises an NMOS transistor resetting the output node of the transmission gate in response to a reset signal.

14. (Previously Presented) The semiconductor memory device of claim 1, wherein the merged output generator comprises;

a NAND gate receiving the first and second path output signals from the first and second path circuits, respectively; and an inverter converting an output of the NAND gate into the merged data bit.

15. (Original) The semiconductor memory device of claim 9, wherein the first edge is a rising edge of the clock signal.

16. (Original) The semiconductor memory device of claim 12, wherein the second edge is a falling edge of the clock signal.

17. (Previously Presented) A semiconductor memory device for operating in a merged data input/output pin (DQ) test mode, comprising:

a control signal generator for generating first and second single data rate (SDR) signals and first and second transmission signal pairs, wherein each signal of a pair is complementary to the other signal of the pair;

a first path circuit for receiving the second single data rate signal and one of the first and second transmission pairs and including a first switching element controlled by the second single data rate signal;

a second path circuit for receiving the first single data rate signal and the other of the first and second transmission pairs and including a second switching element controlled by the first single data rate signal; and

a merged output generator for generating a merged data bit, wherein the merged data bit has an SDR or dual data rate (DDR) pattern depending upon the first single data rate signal fed to the second switching element and the second single data rate signal fed to the first switching element as determined by a respective plurality of output clock signals fed to the control signal generator.

18. (Previously Presented) The semiconductor memory device of claim 17, wherein the merged data bit is generated based on first and second output signals of the first and second path circuits.